PVP 20

Code: 20CS3303

II B.Tech - I Semester –Regular / Supplementary Examinations
DECEMBER 2022

COMPUTER ORGANIZATION AND ARCHITECTURE
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

BL – Blooms Level CO – Course Outcome

			BL	CO	Max. Marks
		UNIT-I			
1	a)	Explain the basic symbols for register transfers with a relevant example.	L2	CO1	4 M
	b)	Draw 4 bit arithmetic logic shift unit and explain same unit in detail.	L3	CO1	10 M
		OR			
2	a)	Construct bus system for four registers with a neat diagram using multiplexers.	L3	CO1	7 M
	b)	Mention the different types of Shifts. Discuss any two types with relevant examples.	L2	CO1	7 M
		UNIT-II			
3	a)	Compare direct and indirect addressing modes.	L4	CO2	7 M

	b)	A computer uses a memory unit with 512K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit. an operation code, a register code part to specify one of 64 registers, and an address part. i) How many bits are there in the operation code, the register code part, and the address part? ii) How many bits are there in the data and address inputs of the memory?	L3	CO2	7 M
OR					
4	a)	List the micro operations for the fetch and decode phases with register transfer statements.	L2	CO3	7 M
	b)	Demonstrate an interrupt cycle with a neat flowchart.	L2	CO3	7 M
UNIT-III					
5	a)	Assume a control word of 14 bits is needed to specify a micro operation in the CPU. List the subtract micro operation for the statement R1 ← R2 - R3.	L4	CO3	7 M
	b)	Demonstrate the organization of a 64 - word register stack	L2	CO3	7 M
OR					

6	a)	Write the assembly code to evaluate the following arithmetic expression: Z=(A-B)*(C/D) i. Using an accumulator type computer with one address instructions ii. Using a stack organized computer with zero address instructions.	L3	CO2	7 M
	b)	Discuss in detail various addressing modes.	L2	CO1	7 M
		UNIT-IV			
7	a)	Apply booth multiplication algorithm to multiply two signed numbers given 12(multiplicand) and -8(multiplier).	L3	CO2	7 M
	b)	Describe in detail associative memory with a neat block diagram.	L2	CO4	7 M
		OR			
8	a)	A block set associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks each of 128 words. i. How many bits are there in each of the TAG, SET and WORD fields? ii. How many bits are there in main memory address.	L3	CO3	7 M
	b)	Explain in detail the relation between address and memory space in a virtual memory system.	L2	CO4	7 M

UNIT-V					
9	a)	Compare and contrast software and hardware priority interrupts.	L4	CO4	7 M
	b)	Derive speed up achieved by a pipeline unit over a non pipeline unit with an example.	L4	CO4	7 M
OR					
10	a)	Compare strobe control and handshaking.	L4	CO4	7 M
	b)	Discuss about instruction pipeline with neat flow chart.	L2	CO4	7 M